EE2401 微算機系統 Fall 2018

HW#3 (8051 Timer, Serial port, Interrupt, Applications) (10/14/2018)

Due date: 11/8/2018. Severe penalty will be given to late homework.

Note:

1. The homework will be graded based on your **documentation** and **demonstration**.
2. For all **(Software Design)** problems, you are required to us **MCU8051IDE**simulators to simulate and verify your programs.
3. You are required to **type** your homework (first the problem then your solution) by using a **word processor** and submit in .doc(or .docx) format under a filename **EE2401f18-hw3-student\_no-vn.doc(or .docx)**, where **student\_no** is your student number, e.g., **106061xxx**(or **X107xxxx**) and **vn** is your version number, e.g., **v3**. You should **upload your .doc file** in **iLMS** by the specified deadline whenever you have a newer version. Follow the iLMS upload homework process to upload your file.
4. The homework will be graded based on your **latest version**. Old version(s) will be discarded.
5. Each homework assignment will have full score of 100 points. 5 points will be deducted if you do not comply with the naming convention. Severe grade penalty will be given to late homework. 5 points will be taken off per day after deadline.
6. Please treat the above requirements as a kind of training in writing a decent homework report. If you have any problem regarding this homework, please feel free to consult with TA or me. If you think the time is too short to accomplish this homework, please let me know in class.

1. (Software Design) (30%)

Serial communication

1. Write a main program that will first initialize the 8051 serial port in **mode 1** with 9600 baud, odd parity, non-interrupt-driven, and then call a subroutine called **INLINE** to read from serial port a line of ASCII codes terminated with a carriage return character code (0DH) and store it in a line buffer with an extra null character (00H) for its termination. It will then call a subroutine **OUTSTR** to send out the received line in the line buffer via serial port. Assume the line buffer is residing in the **external data memory** beginning at address **60H**with the length of the line buffer limited to 40 bytes. When calling both subroutines, the **R0** is used as the pointer to the line buffer.
2. Repeat (a) with serial port enabled in interrupt-driven mode.

2. (Hardware schematic design and software design)(30%)

I/O expansion using **shift registers of serial por**t

We want to use serial port in **mode 0** to expand 8051 I/O pins. Assume that we want to have 16 extra output pins with each bit value stored in bit-addressable memory 20H, 21H and 16 extra input pins read into bit-addressable memory 22H, 23H using serial-in-parallel-out and parallel-in-serial-out shift registers connected to 8051 serial port for I/O expansion, respectively. The I/O pins should be updated at least 100 times per second.

1. Please pick the proper TTL shift registers and ICs whenever needed, study their datasheets, and draw a simplified schematic diagram showing the necessary connection of them with 8051.
2. Design an 8051 program for fulfilling this task by first designing your flow chart, examining its logical validity, then designing the codes.

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Parallel-in serial-out

Serial-in parallel-out

Tx

Rx

16 inputs

16 outputs

8051

3. (Hardware and software design) (40%)

I/O expansion using **multiprocessor communication**

8051 Slave 1

P0 P1 P2

Tx Rx

8051 Slave 2

P0 P1 P2

Tx Rx

8051 Slave 3

P0 P1 P2

Tx Rx

8051 Slave 4

P0 P1 P2

Tx Rx

Tx

Rx

8051 Master

As shown above, we have an 8051 master and 4 8051slaves connected in multiprocessor communication configuration using serial ports. Each slave has its id as shown. Slave 1 and 2 provide 6 x 8 = 48 input pins; slave 3 and 4 provide 48 output pins.The states of those 96 I/O pins are to be stored at master’s bit-addressable memory starting at bit address 00H ~ bit address 5FH (i.e., byte address 20H ~ 2BH). Please design codes for master and each slave (slave 1 and 2 may have similar code, so do slave 3 and 4) to fulfill the task. You should provide:

* a subroutine to initialize master and slave 8051’s and configure the input, output ports,
* a subroutine to read in all input ports and placed them in master’s internal bit-addressable bits,
* a subroutine to output from masters bit-addressable bits to slave 3 and 4 ports, and
* a main program that can continuously handle those I/O pins.

1. Design flowcharts or pseudo codes for Init subroutine, Input subroutine, and Output subroutine for 8051 master and slaves.
2. Finally, based on (a), design the main and serial port programs for the master and each slave 8051s.